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IMPROVED FLIP CHIP BALL GRID ARRAY PACKAGE

FIELD OF THE INVENTION

[0001] This is a continuation-in-part of United States patent application serial no. 10/211,567 entitled Improved Chip Scale Integrated Circuit Package, filed August 5, 2002, mow PAT 6, 667, 191.

FIELD OF THE INVENTION

[0002] The present invention relates in general to integrated circuit packaging, and more particularly to a flip chip ball grid array package with improved thermo-mechanical properties.

BACKGROUND OF THE INVENTION

[0003] High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by industry demands for increased thermal and electrical performance and decreased size and cost of manufacture

[0004] In general, array packaging such as Ball Grid Array (BGA) packages provide a high density of interconnects relative to the surface area of the package. Typical BGA packages include a convoluted signal path, giving rise to high impedance and an inefficient thermal path which results in poor thermal dissipation performance. With increasing package density, the spreading of heat generated by the device is increasingly important.

[0005] Direct connection of the semiconductor die to a substrate surface in a flip-chip orientation, using solder ball connections provides low impedance packages relative to the use of wire-bond connections and provides reduced package space. This technology is becoming increasingly popular with package fabrication advances including advances in forming and placing of solder balls in flip-chip packaging.

[0006] Figure 1 shows a sectional view of a conventional flip-chip BGA package indicated generally by the numeral 20. The flip-chip BGA package includes a substrate 22 with a semiconductor die 24 mounted in a flip-chip orientation, to a first surface of the substrate 22. Solder balls 26 provide electrical connections between the semiconductor die 24 and the substrate 22. Solder balls 28, in the form of a ball grid array are disposed on the second